

General Description

The MP7781 is an 80W Class D Audio Amplifier. It is a fully integrated audio amplifier, which dramatically reduces solution size by integrating the following:

- **Start-up / Shut-Down Pop Elimination**
- **Low Quiescent Current**
- **Short Circuit Protection**
- **Mute / Standby Mode**
- **105mΩ Power MOSFETs**

The MP7781 utilizes a full bridge output structure capable of delivering 80W into 4Ω speakers. It uses Monolithic Power Systems' proprietary Analog Digital Adaptive Modulation (ADAM™) to convert the audio input signal into pulses. As in all other MPS Digital Audio Amplifiers, this device exhibits the high fidelity of a Class AB amplifier at efficiencies greater than 90%. The MP7781 is packaged in a standard SOIC24 package with an exposed pad allowing for top mounted heat sinks. The MP7781 is US Patent Pending.

Ordering Information

Part Number*	Package	Temperature
MP7781EWR	SOIC24WR	-20°C to +85°C

* For Tape & Reel, use suffix -Z (MP7781EWR-Z)

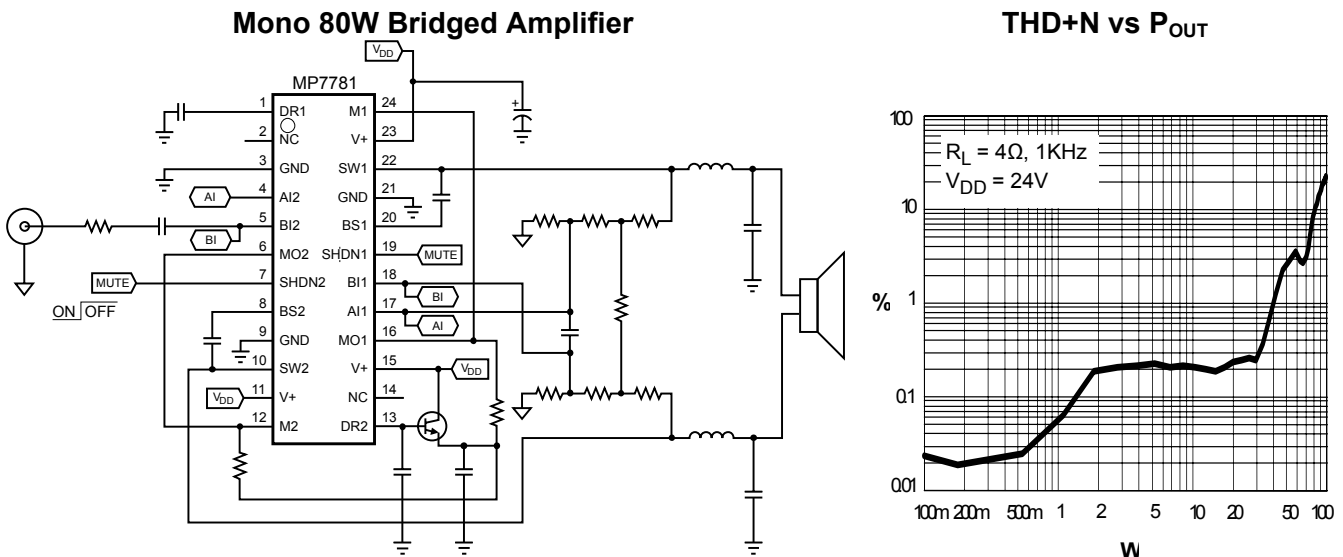
Features

- 80W into 4Ω with 24V Input
- 95% Efficiency at 80W
- Amplifies Full Audio Range with THD+N Typical = 0.2%
- 7.5V to 24V Operation
- Full Bridge Output Drive
- 4 Integrated 105mΩ Switches
- Turn-on / Turn-off Click and Pop Elimination
- Integrated Short Circuit Protection
- Integrated Thermal Shutdown
- Mute / Standby Mode
- Exposed Pad on Top Surface for Mounting Heat Sink

Applications

- Amplified Speakers
- Amplified Subwoofers
- Multimedia Computers
- Televisions
- Monitors
- Home Theatre Systems
- DVD and VCD Players
- Game Devices and Systems

Typical Application



Initial Release

Absolute Maximum Ratings (Note 1)

Supply Voltage (V+)	26V
PGND to AGND	-0.3V to 0.3V
BST to SW Voltage	-0.3V to 6V
SHDN Voltage (V _{SHDN})	-0.3V to 6V
M1, M2 Voltage	6V
V _{AI} , V _{BI}	-1V to V+ +1V
Junction Temperature	150°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V+)	7.5V to 24V
Operating Temperature	-20°C to +85°C

Package Thermal Characteristics (Notes 3 & 4)

Thermal Resistance θ_{JA}	36°C/W
Thermal Resistance θ_{JC}	3°C/W

Electrical Specifications (Circuit of Figure 1, V_{DD}=24V, unless otherwise specified, T_A=25 °C)

Parameters	Condition	Min	Typ	Max	Units
V+ Quiescent Current	No Load, V _{SHDN} = 0V		8		mA
SW On Resistance (Note 5)	V+ = 7.5V to 24V		105		mΩ
SW Short Circuit Current			9		A
AI, BI Input Common Mode Voltage Range		0		V+ - 2	V
AI, BI Input Current	V _{AI} = V _{BI} = 12V		100		μA
SHDN Input Threshold Voltage	V _{SHDN} Rising	2	1.4		V
	V _{SHDN} Falling		1.2	0.4V	V
SHDN Input Current	V _{SHDN} = 5V		1		μA
Thermal Shutdown (Note 5)	T _J Rising		160		°C
Thermal Hysteresis (Note 5)			20		°C

Operating Specifications (Circuit of Figure 1, V_{DD} = 24V, R_L = 4Ω unless otherwise specified, T_A = 25 °C)

Parameters	Condition	Min	Typ	Max	Units
Power Output	f = 1KHz @ 10% THD+N		80		W
	R _L = 8Ω		45		W
Total Harmonic Distortion + Noise	P _{OUT} = 10W, f = 1KHz		0.2		%
Efficiency	f = 1KHz, P _{OUT} = 10W		95		%
Maximum Power Bandwidth	-3dB point		20		KHz
Dynamic Range			90		dB
Noise Floor	A-Weighted, 22KHz BW		100		μV
Power Supply Rejection	f = 100Hz		80		dB

Notes:

1. Exceeding these limits may damage the device.
2. The device is not guaranteed to function outside of its operating range.
3. Measured on one square inch copper clad FR4 board.
4. θ_{JC} is Junction to Exposed Pad.
5. Guaranteed by design, not tested.

Pin Description

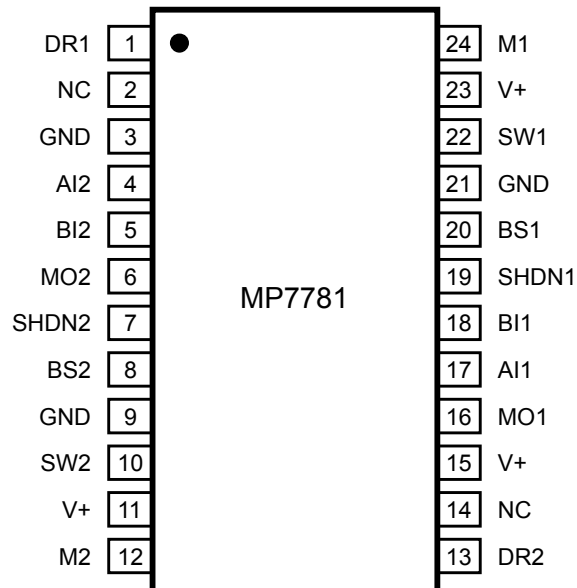


Table 1: Pin Functions

Pin #	Pin Name	Pin Function
1	DR1	Ch 1 Low-Side Drive Regulator output. Supplies the gate drive current to the Low-side DMOS for the Ch 1 output. Connect a 0.1 μ F to 1 μ F cap from DR1 to GND. Do not connect to DR2
2	NC	No Connection. Recommend connect to the Pin 1 or Pin 3.
3	GND	Internal Modulator Ground. Connect GND to the power ground plane. Connect the power ground plane to the analog ground plane at a single point.
4	AI2	Negative feedback of Ch 1.
5	BI2	Negative feedback of Ch 2 and audio input.
6	MO2	Internal Modulator Ch 2 PWM Output. Open drain type output connecting to Ch 2 Driver input M2 Pin 26. Use a Pull up resistor to 5V.
7	SHDN2	Enable Input. Drive SHDN2 low to turn-on the amplifier, drive it high to turn-off. Connect both SHDN inputs (pin 7 and pin 19) together externally.
8	BS2	Ch 2 High-Side MOSFET Bootstrap Input. A capacitor from SW2 to BS2 supplies the gate drive current to the high-side MOSFET for Ch 2 Output. Connect a 0.1 μ F to 1 μ F cap.
9	GND	Ch 2 Power Ground. Connect GND to the power ground plane. Connect the power ground plane to the analog ground plane at a single point.
10	SW2	Ch 2 Switched Power Output. SW2 is the output of Ch 2. Connect the LC filter between SW2 and the negative side of the load.

Table 1: Pin Functions (cont.)

Pin #	Pin Name	Pin Function
11	V+	Power Supply Input. V+ is the drain of high-side MOSFET switch, and supplies the power to output stage and internal control circuitry. Bypass V+ to GND with a 1 μ F or greater cap.
12	M2	Ch 2 PWM Input. 5V Digital input to Ch 2 Driver. Use a Pull up resistor to 5V Also connecting to MO2 Pin 6.
13	DR2	Ch 2 Low-Side Drive Regulator output. Supplies the gate drive current to the Low-side DMOS for the Ch 2 output. Connect a 0.1 μ F to 1 μ F cap from DR2 to GND. Do not connect to DR1
14	NC	No Connection. Recommend connect to the Pin15.
15	V+	Internal Modulator Power Supply Input. Bypass V+ to GND with a 1 μ F or greater capacitor.
16	MO1	Internal Modulator Ch 1 PWM Output. Open drain type output connecting to Ch1 Driver input M1 Pin1. Use a Pull up resistor to 5V.
17	A11	Negative feedback of Ch 1.
18	BI1	Negative feedback of Ch 2 and audio input.
19	SHDN1	Enable Input. Drive SHDN1 low to turn-on the amplifier, drive it high to turn-off. Connect both SHDN inputs (pin 7 and pin 19) together externally.
20	BS1	Ch 1 High-Side MOSFET Bootstrap Input. A capacitor from SW1to BS1 supplies the gate drive current to the high-side MOSFET for the Ch 1 output. Connect a 0.1 μ F to 1 μ F cap.
21	GND	Ch 1 Power Ground. Connect GND to the power ground plane. Connect the power ground plane to the analog ground plane at a single point.
22	SW1	Ch 1 Switched Power Output. SW1 is the output of Ch 1. Connect the LC filter between SW1 and the positive side of the load.
23	V+	Power Supply Input. V+ is the drain of high-side MOSFET switch, and supplies the power to output stage and internal control circuitry. Bypass V+ to GND with a 1 μ F or greater cap.
24	M1	Ch 1 PWM Input. 5V Digital input to Ch 1 Driver. Use a Pull up resistor to 5V Also connecting to MO1 Pin 16.

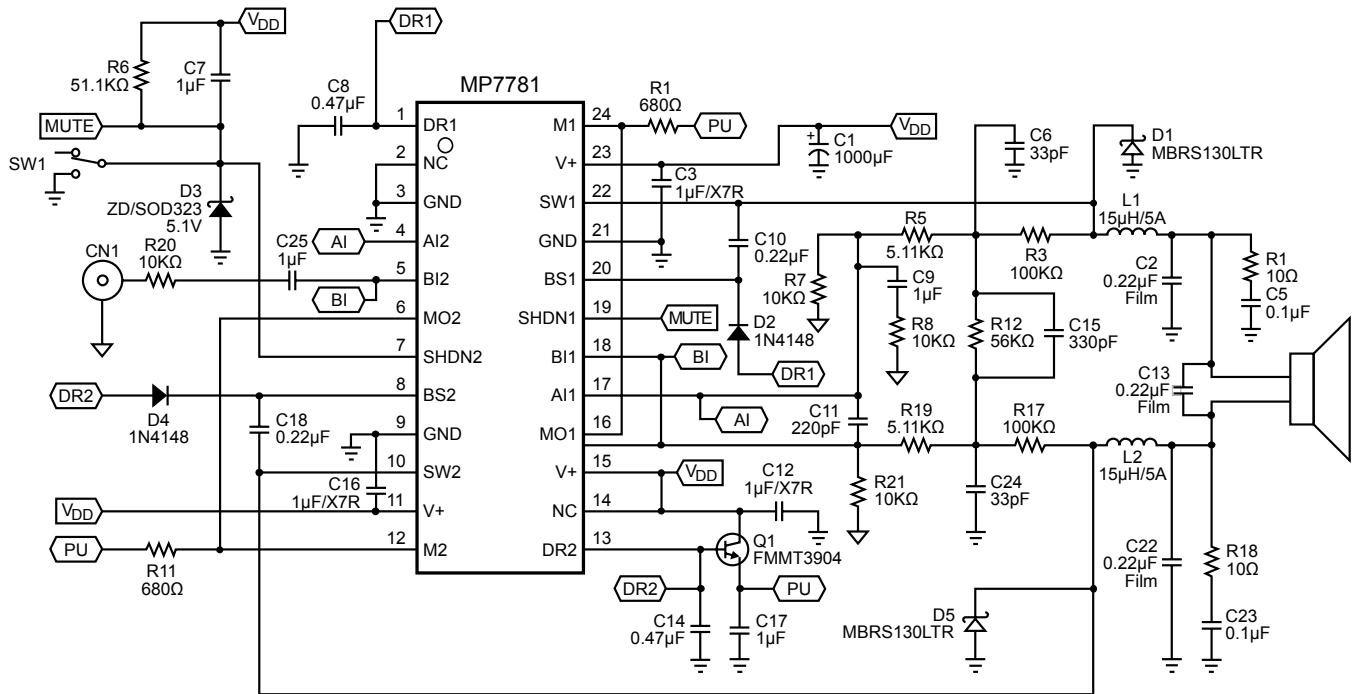


Figure 1: Mono Full Bridge Circuit

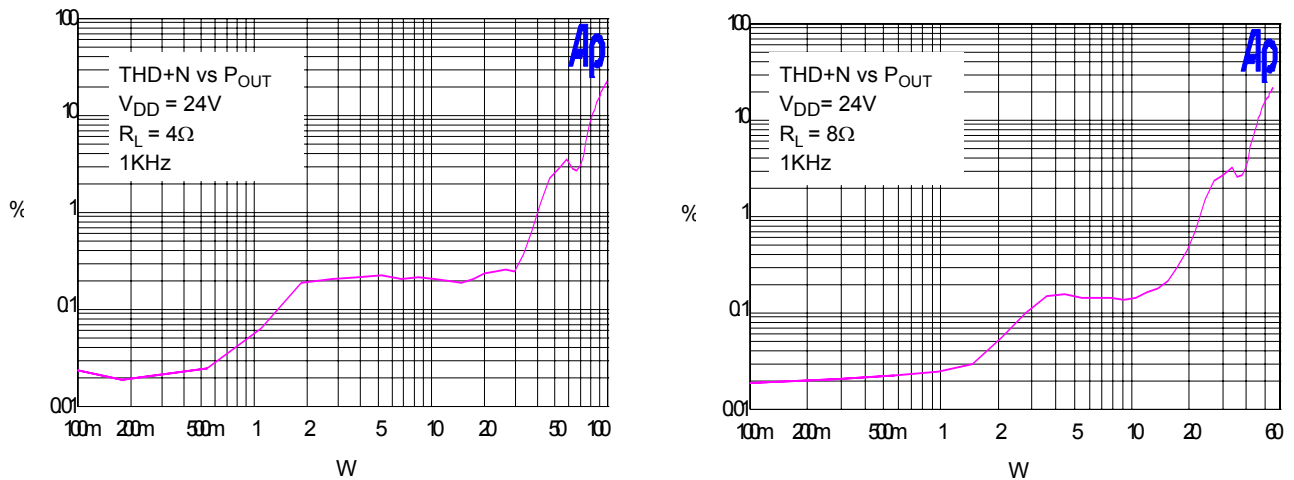
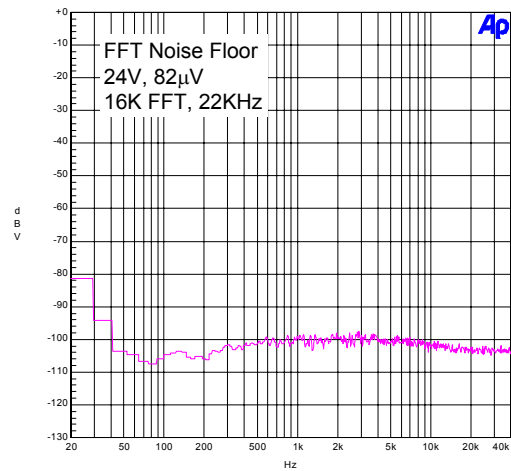
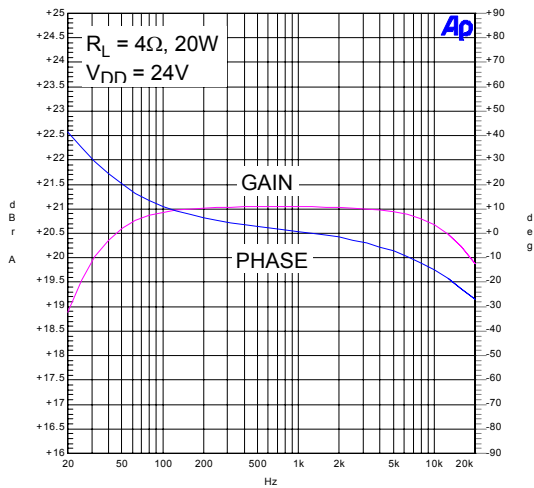
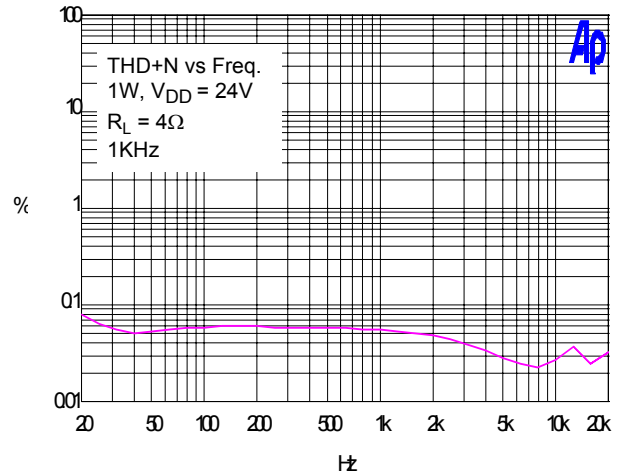
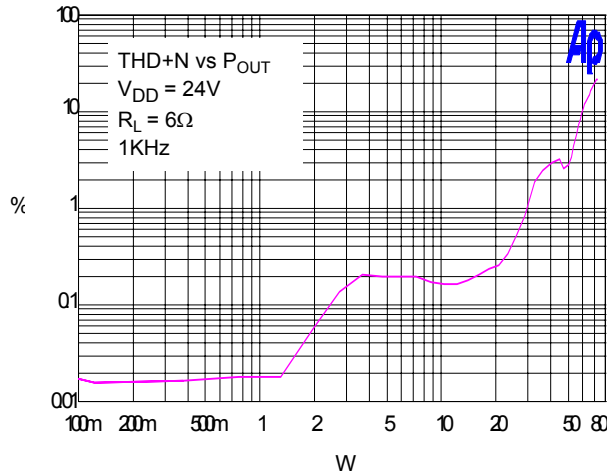


Figure 2: Typical Operating Characteristics (Circuit of Figure 1, $V_{DD}=24V$, $T_A=25^\circ C$)



Efficiency Vs Output Power

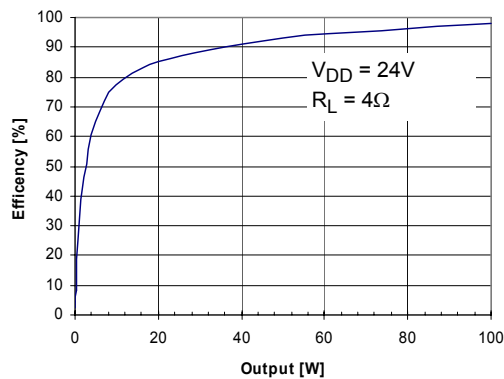


Figure 2 (cont.): Typical Operating Characteristics (Circuit of Figure 1, $V_{DD}=24V$, $T_A=25^\circ C$)

Functional Description

The MP7781 is an 80W bridge-connected Class D audio amplifier. It uses the Monolithic Power Systems' proprietary Analog Digital Adaptive Modulation (ADAM™) to convert the audio input signal into pulses. It then drives the power output stage that is filtered through an external inductor-capacitor filter to drive the load. Because of the switching output stage, power dissipation in the amplifier is drastically reduced compared to Class-AB amplifiers while maintaining high fidelity and low distortion.

The amplifier uses a differential input to the modulators. AI1 and AI2 are the positive inputs and BI1 and BI2 are the negative inputs, as shown in Figure 1. The input capacitor C25 blocks DC current at the input. The resistors, R12, R3, R5, R7, R17, R19, and R21, set the quiescent output voltage of each side of the speaker terminal voltage to the $V_{DD}/2$.

The amplifier voltage gain is set by the combination of R20, R3, R5, R7, R17, R19, R21, and R12. The circuit of Figure 1 produces both side with a voltage gain of 10 V/V. Since channel 1 and channel 2 are 180° out of phase, the total amplifier voltage gain is:

$$A_V(\text{total}) = 2 \times A_V(\text{preamp}) \times A_V(\text{power})$$

Where A_V total is the total voltage gain, A_V power is the voltage gain of a single channel of the MP7781. The circuit of Figure 1 produces a overall voltage gain of 20. This is suitable for a 1Vrms input signal and $V_{DD} = 24V$, with some clipping at the highest output power level.

Application Information

The MP7781 uses a minimum number of external components to complete a Digital audio amplifier. The circuit of Figure 1 is optimized for a 24V power supply and a 1V RMS input signal.

The output driver stage uses four 105mΩ n-channel MOSFETs to deliver the pulses to the LC output filters which in turn drive the load. To fully enhance the high-side MOSFETs, the gates are driven to a voltage higher than the sources by the bootstrap capacitors. While the output is driven low, the bootstrap capacitors are charged from V_{DD} through an internal circuit of the MP7781. When the MOSFETs are driven high, the gates are driven from the voltage at BS1 and BS2, forcing the MOSFET gates to a voltage higher than V_{DD} , allowing the MOSFETs to be turned on fully, thus reducing power loss in the amplifier.

Short Circuit / Overload Protection

The MP7781 has internal overload and short circuit protection. The currents in both the high-side and low-side MOSFETs of each output are measured. If the current on any channel exceeds the 9A short circuit current limit, both MOSFETs of that channel are turned off, allowing the inductor current to decay to 0. Then the MP7781 restarts with the same power up sequence that is used for normal starting to prevent a pop from occurring after a short circuit condition is removed.

Mute / SHDN Function

The MP7781 is disabled by driving the SHDN input High, and it is enabled by driving it Low. While the MP7781 is disabled, the V_{DD} operating current drops below 10mA and the output driver MOSFETs are turned off.

This circuit is suitable for most applications. If this circuit is not suitable, use the following sections to determine how to customize the amplifier for a particular application.

Setting the Voltage Gain

The voltage gain sets the output voltage swing for a given input voltage swing. The output voltage swing is limited by the power supply, since it can not swing above the power supply voltage or below ground. To achieve the maximum power out of the MP7781 amplifier, set the gain such that the maximum input signal results in the maximum output voltage swing. In some cases, some output voltage clipping is allowed at the maximum output levels. In this case, increase the voltage gain from the unclipped value by as much as 30%.

The maximum unclipped output voltage swing is $\pm V_{DD}$. For a given input signal voltage, where $V_{IN(pk)}$ is the peak input voltage, the maximum unclipped voltage gain is:

$$A_V(\text{max}) = \frac{V_{DD}}{V_{IN(pk)}}$$

Setting the Switching Frequency

The switching frequency is set by the capacitor C11. Lower switching frequencies result in more inductor ripple, causing more quiescent output voltage ripple, increasing the output noise distortion. Higher switching frequencies result in more power loss. Usually the minimum switching frequency should be 10 times higher than the maximum audio frequency. The optimum quiescent switching frequency is approximately 400kHz.

Choosing the LC Filter

The Inductor-Capacitor (LC) filter converts the pulse trains at SW1 and SW2 to the output voltage that drives the speaker. Typical values for the LC filter are shown in Figure 1, L1 and L2 = 15 μ H inductor and C2, C22, and C13 = 0.22 μ F.

The characteristic frequency of the LC filter needs to be high enough to allow high

frequency audio to the output, yet needs to be low enough to filter out high frequency products of the pulses from SW. The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

The quality factor (Q) of the LC filter is important. If this is too low, output noise increases. If the Q is too high, then peaking may occur at high signal frequencies reducing the bandpass flatness. The circuit Q is set by the load resistance (speaker resistance, typically 4 Ω). The Q is calculated as:

$$Q = \frac{R}{\sqrt{\frac{L}{C}}}$$

Use an LC filter with Q between 0.7 and 2

The actual output ripple and noise is greatly affected by the type of inductor and capacitor used in the LC filter. Use a film capacitor and an inductor with sufficient power handling capability to supply the output current to the load. The inductor should exhibit soft saturation characteristics. If the inductor exhibits hard saturation, it should operate well below the saturation current. Gapped ferrite, MPP, Powdered Iron, or similar type toroidal cores are recommended. If open or shielded bobbin ferrite cores are used, make sure that the start windings of each inductor line up (all starts going toward SW pins, or all starts going toward the output) to prevent crosstalk or other channel-to-channel interference.

Input Blocking Capacitor

The input blocking capacitor, C1, is used to block DC currents at the input. The source input signal is typically centered around the circuit ground, but the MP7781 inputs are at half the power supply voltage ($V_{DD}/2$). The input blocking capacitor transmits the signal from the source to the MP7781 input while blocking the DC voltage. The input capacitor forms a high-pass filter with the input resistor R20. Choose the value of the input blocking capacitor such that the corner frequency (f_{IN}) of this filter is less than the minimum required audio frequency. The input corner frequency is calculated by the following:

$$f_{IN} = \frac{1}{2\pi \times R20 \times C25}$$

Use a ceramic capacitor for C1. Make sure that the dielectric changes little with capacitor bias voltage. Use NPO, X7R, X5R or equivalent type capacitors.

Power Source

For maximum output power, the amplifier circuit requires a regulated external power source to supply the power to the amplifier. The higher the power supply voltage, the more power can be delivered to a given load resistance. However, if the voltage exceeds the maximum operating voltage of 24V, the MP7781 may sustain damage.

The power source must be able to source the peak load current. The power supply rejection of the MP7781 is excellent (80dB typ.), however, noise at the power supply can get to the output. Care must be taken to minimize power supply noise within the audio frequencies. Bypass the power supply with a large value capacitor (typically aluminum electrolytic or tantalum) along with a smaller 1 μ F or greater ceramic capacitor at both pin 11 and pin 23 of the MP7781 V_{DD} inputs.

Circuit Layout

The circuit layout is critical for optimum performance and low output distortion and noise. Place the following components as close to the MP7781 as possible:

1. **Power supply bypass, C7, C9.** C7 and C9 carry the transient current for the switching output stages. To prevent overstressing of the MP7781 and excessive noise at the output, place the power supply bypass capacitors as close to V_{DD} and PGND as possible.
2. **Output Catch Diodes, D1, D5.** D1 and D5 carry the current over the dead-time while all MOSFET switches are off. Place the diodes between SW and PGND to prevent the voltage at SW from swinging excessively below ground.
3. **Integrator Capacitors, C11** is used to set the amplifier switching frequency. Place the capacitors as close to the differential input pins (AI and BI) as possible to reduce distortion and noise.

Use two separate ground planes, analog ground (AGND) and power ground (PGND), and connect the planes together at a single point to prevent noise injection into the amplifier input and to reduce distortion.

Analog components (R7, R8, R21, and the input source ground) connect to the analog ground. Place the sense resistors (R3, R5, R7, R17, R19, R21, and R12) as close to each other. Place the input resistor and capacitor (R20 and C25) as close to the BI inputs as possible. Make sure that any traces carrying the switching node (SW) voltages are far from the input signal. If it is required to run the SW trace near the input, shield the input with a ground plane between the traces. Make sure that all inductors used on a single circuit board have the same orientation.

Power components connect to power ground. If multiple amplifiers are used on a single board, make sure that each channel is physically separated to prevent crosstalk and make sure that the power supply is routed from the source to each channel individually, not serially to prevent channel-to-channel coupling through the power supply input.

Electro-Magnetic Interference (EMI)

Due to the switching nature of the Digital amplifier, care must be taken to minimize the effects of electromagnetic interference from the amplifier to other sensitive circuitry within the system.

The size of high-current loops that carry rapidly changing currents needs to be minimized. To

do this, make sure that the V_{DD} bypass capacitors (C3, C12, C16, C8, C10, C14, and C18) are as close to the MP7781 as possible.

Nodes that carry rapidly changing voltage, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

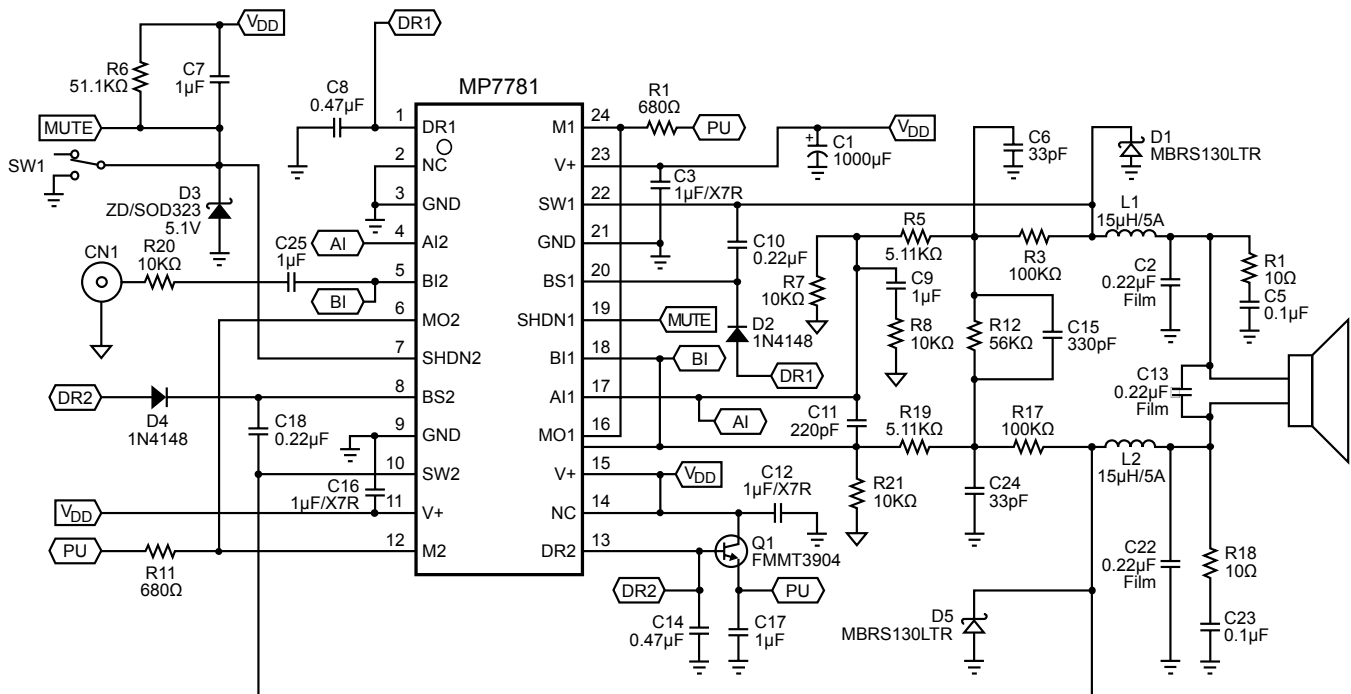
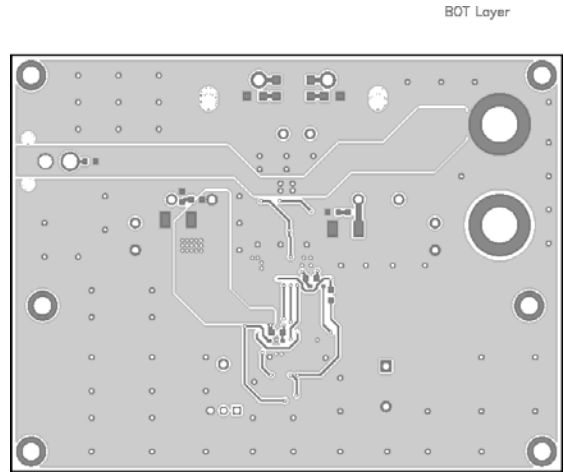
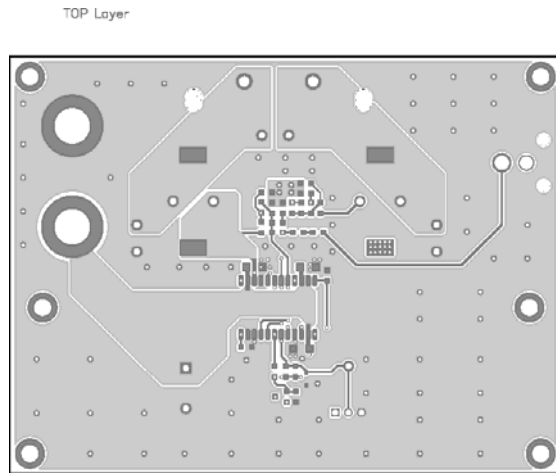


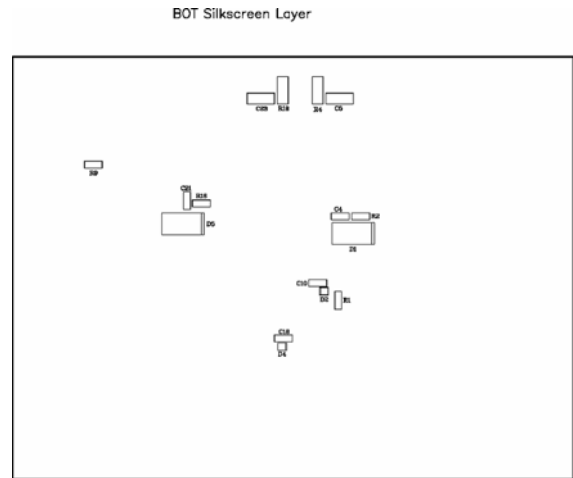
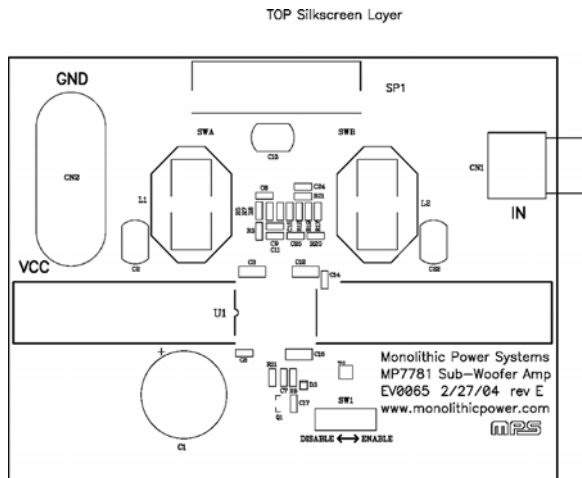
Figure 3: Simplified Single-Channel Full-Bridge Circuit (for MPS Evaluation Board EV0065)



Pattern Top

Pattern Bottom

Figure 4a: EV0065 Printed Circuit Board Layout



Silkscreen Top

Silkscreen Bottom

Figure 4b: EV0065 Printed Circuit Board Layout

EV0065 Bill of Materials

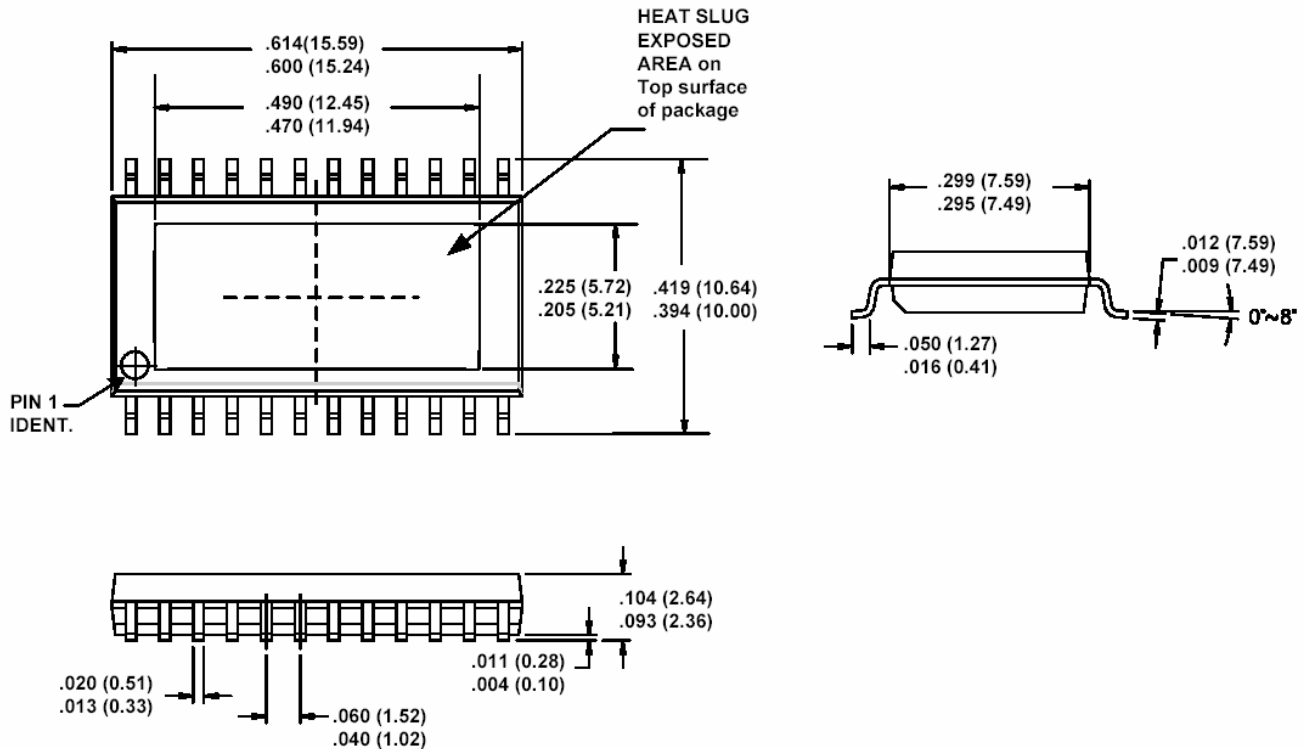
BOM Item	Qty	Ref Des	Value	Description	Package	Manufacturer	Manufacturer Part Number
1	2	C10	0.22 μ F	Ceramic Cap, 25V, X7R	SM0805	Panasonic	ECJ-2YB1E224K
		C18					
2	4	C7	1 μ F	Ceramic Cap, 16V, X5R	SM0805	Panasonic	ECJ-2FB1C105K
		C9					
		C17					
		C25					
3	1	C11	220pF	Ceramic Cap, 50V, X7R	SM0805	Panasonic	ECU-V1H221KBN
4	2	C6	33pF	Ceramic Cap, 50V, NPO	SM0805	Panasonic	ECJ-2VC1H330J
		C24					
5	2	C8	0.47 μ F	Ceramic Cap, 16V, X7R	SM0805	Panasonic	ECJ-2YB1C474K
		C14					
6	3	C3	1 μ F	Ceramic Cap, 25V, X7R	SM1206	Panasonic	ECJ-3YB1E105K
		C12					
		C16					
7	2	C4	390pF	Ceramic Cap, 50V, X7R	SM0805	Panasonic	ECU-V1H391KBN
		C21					
8	1	C15	330pF	Ceramic Cap, 50V, X7R	SM0805	Panasonic	ECU-V1H331KBN
9	1	C1	1000 μ F	Electrolytic Cap, 25V, FC	Radial	Panasonic	EEU-FC1E102S
10	3	C2	0.22 μ F	Film Cap, 50V	Radial	Panasonic	ECQ-V1H224JL
		C13					
		C22					
11	2	C5	0.1 μ F	Ceramic Cap, 50V, X7R	SM1206	Panasonic	ECJ-3VB1H104K
		C23					
12	1	D3		Diode Zener, 5.1V, 200mW	SOD323	Diodes Inc	BZT52C5V1S-7
13	2	D1		Diode Schottky, 30V, 1A	SMB	IRF	MBRS130LTR
		D5					
14	2	D2		Diode Switch, 75V, 400mW	SOD-123	Diodes Inc	1N4148W-7
		D4					
15	2	L1	15 μ H	Inductor Power, 5A, 16RHBP	Radial	Toko	
		L2					
16	1	U1		Class D Amplifier	SO24	MPS	MP7781
17	1	CN1		Connector RCA Jack, RA		CUI Inc	RCJ-041

EV0065 Bill of Materials (cont.)

BOM Item	Qty	Ref Des	Value	Description	Package	Manufacturer	Manufacturer Part Number
18	2	R2	10Ω	Film Res, 5%	SM0805	Panasonic	ERJ-6GEYJ100V
		R16					
19	2	R4	10Ω	Film Res, 5%	SM1206	Panasonic	ERJ-8GEYJ100V
		R18					
20	2	R5	5.11KΩ	Film Res, 1%	SM0805	Panasonic	ERJ-6ENF5111V
		R19					
21	2	R8	10KΩ	Film Res, 5%	SM0805	Panasonic	ERJ-6GEYJ103V
		R20					
22	2	R7	10KΩ	Film Res, 1%	SM0805	Panasonic	ERJ-6ENF1002V
		R21					
23	1	R6	51.1KΩ	Film Res, 1%	SM0805	Panasonic	ERJ-6ENF5112V
24	1	R12	56KΩ	Film Res, 1%	SM0805	Panasonic	ERJ-6ENF5602V
25	2	R3	100KΩ	Film Res, 1%	SM0805	Panasonic	ERJ-6ENF1003V
		R17					
26	2	R1	680Ω	Film Res, 5%	SM0805	Panasonic	ERJ-6GEYJ681V
		R11					
27	1	R9	1KΩ	Film Res, 5%	SM0805	Panasonic	ERJ-6GEYJ102V
28	1	Q1		Transistor, NPN, 40V, 200mA	SOT-23	Zetex Inc	FMMT3904TA
29	1	SP1		Speaker Connector, 2-Pin			
30	1	SW1		Switch SPDT, PC Mount		E-Switch Inc	EG1218
31	1	CN2		Connector Jack Banana			

Packaging Information

SOIC24 (Exposed Pad - Reverse Bond)



NOTE:

- 1) Control dimension is in inches. Dimension in bracket is millimeters

NOTICE: MPS believes the information in this document to be accurate and reliable. However, it is subject to change without notice. Please contact the factory for current specifications. No responsibility is assumed by MPS for its use or fit to any application, nor for infringement of patent or other rights of third parties.